(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 489 623 A1

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
22.12.2004 Bulletin 2004/52

(51) Int Cl.[7]: **G11C 11/56**, G11C 11/34

(21) Application number: **03026610.0**

(22) Date of filing: **19.11.2003**

(84) Designated Contracting States:
AT BE BG CH CY CZ DE DK EE ES FI FR GB GR HU IE IT LI LU MC NL PT RO SE SI SK TR
Designated Extension States:
AL LT LV MK

(30) Priority: **18.06.2003 US 465012**

(71) Applicant: **Macronix International Co., Ltd.**
Hsinchu (TW)

(72) Inventors:
- **Chen, Yi-Chou**
  Hsinchu (TW)
- **Lu, Chih-Yuan**
  Hsinchu (TW)

(74) Representative: **Becker Kurig Straus**
Patentanwälte
Bavariastrasse 7
80336 München (DE)

(54) Multi-level memory device and methods for programming and reading the same

(57) A multilevel memory core includes a word line and a bit line. The multilevel memory core also includes a core cell in electrical communication with the word line and the bit line. The core cell includes a threshold changing material. The threshold changing material is programmed to define multiple levels for storage where each of the multiple levels for storage is associated with a corresponding threshold voltage. Methods for reading the multilevel memory core also are described.

EP 1 489 623 A1

Printed by Jouve, 75001 PARIS (FR)

Description

BACKGROUND OF THE INVENTION

[0001] The present invention relates generally to memory devices and, more particularly, to a method of programming a threshold changing material of a memory cell to allow for multilevel data storage and associated reading techniques.

[0002] The resistance ratio of amorphous and crystalline chalcogenide is typically more than 1000 times. Due to this difference it has been proposed to separate the resistance into several stages and utilize the stages for are multi-level storage. Figure 1 is a graph illustrating a plot of the resistance versus the current for a multi-level chalcogenide random access memory (RAM). As is illustrated by line 102, the resistance steps up according to each current increment. The resistance of chalcogenide may be tuned, however, one of the shortcomings associated with defining the stages through the resistance is that the resistance difference is difficult to sense because the sensing margin is small for multi-level applications and the sensing time for the high resistance stage will be long. For example, assuming that there are 4 states of resistance and they are 5k, 50k, 500k and 5M Ohm, the current to read a cell is usually 20 μA. If we apply 0.1 V on a cell, and the cell resistance may be 5k, 50k, 500k and 5M, the current read will be 20 μA, 2 μA, 0.2 μA (which can be hardly sensed), and 20 nA (the same order as noise), respectively. That is, it is almost impossible to sense all the states at that level.

[0003] In light of the foregoing, there is a need for a multi-level (multiple bits per cell) memory cell structure that includes a feature that is readily sensed for the multiple levels so that the associated states may be easily discerned.

SUMMARY OF THE INVENTION

[0004] Broadly speaking, the present invention provides a memory cell structure that is capable of defining multiple bits per cell through the use of a threshold changing material.

[0005] In accordance with one aspect of the present invention, a multilevel memory core is provided. The multilevel memory core includes a word line and a bit line. A core cell in electrical communication with the word line and the bit line is also included. The core cell includes a threshold changing material. The threshold changing material is programmed to define multiple levels for storage where each of the multiple levels for storage is associated with a corresponding threshold voltage.

[0006] In one embodiment, the threshold changing material is programmed by applying different energy pulses to the threshold changing material. In another embodiment, the voltage threshold is tuned through the application of the different energy pulses.

[0007] In accordance with another aspect of the present invention, a method for reading a multilevel memory device is provided. The method includes applying a read voltage to the multilevel memory device. Then, a state of a current associated with the read voltage is determined. Next, an access state of the multilevel memory device based on the current is determined.

[0008] In one embodiment, the multilevel memory device is programmed prior to being read. The programming includes tuning a voltage threshold through the application of varying energy pulses.

[0009] In accordance with yet another aspect of the present invention, a method for reading multiple levels of a multilevel memory device is provided. The method initiates with applying a voltage to a threshold changing material of the multilevel memory device. Then, a current related to the voltage is sensed to distinguish between each of the multiple levels.

[0010] It will be apparent to those skilled in the art that the method of reading the multilevel memory device of the present invention may be applied in numerous memory/solid state device applications. One of the significant advantages of the read method is the speed and the sensing margin achieved when reading the current as opposed to sensing resistance.

[0011] It is to be understood that the foregoing general description and the following detailed description are exemplary and explanatory only and are not restrictive of the invention, as claimed.

BRIEF DESCRIPTION OF THE DRAWINGS

[0012] The accompanying drawings, which are incorporated in and constitute part of this specification, illustrate exemplary embodiments of the invention and together with the description serve to explain the principles of the invention.

Figure 1 is a graph illustrating a plot of the resistance versus the current for a multi-level chalcogenide random access memory (RAM).

Figure 2 is a simplified schematic diagram of a portion of a typical chalcogenide memory array.

Figure 3 is a normalized current (I)-normalized voltage (V) curve where different programming pulses were applied to applied to a threshold changing material in order to define different threshold voltages.

Figure 4 is a flow chart diagram illustrating the method operations for reading the multi-level states associated with a threshold changing material.

Figure 5 is flowchart diagram representing an alternative method for reading the multi-level states of a threshold changing material described with reference to Figure 4.

DETAILED DESCRIPTION OF EXEMPLARY EMBODIMENTS

[0013] Several exemplary embodiments of the invention will now be described in detail with reference to the accompanying drawings. Figure 1 has been described above in the "Background of the Invention" section.

[0014] In accordance with the present invention, a threshold voltage associated with a threshold changing material is obtained by applying different energy pulses in order to define different threshold voltages. In one embodiment, the threshold changing material is a chalcogenide material. Further information on adjusting the threshold voltage, V_{th}, of a material capable of changing V_{th} is discussed in related U.S. Patent Application No. _____(Attorney Docket No. MXICP020), filed on even date herewith, and entitled " Method for Adjusting the Threshold Voltage for a Memory Cell.". The disclosure of this related application is incorporated herein by reference for all purposes. Above the threshold voltage, the current associated with each stage is distinguishable. Consequently, by sensing the current, the corresponding states may be determined. Therefore, within one memory core cell multiple states may exist and the different states correspond to a sensed current.

[0015] Figure 2 is a simplified schematic diagram of a portion of a typical chalcogenide memory array. Memory array portion 112 includes word lines 108 a and 108b, bit lines 110a and 110b, transistor device 104, and chalcogenide device 106. Transistor device 104 functions as a steering device, i.e., an access transistor, which provides access to chalcogenide device 106 from the corresponding word line and bit line. By way of example, transistor device 104 may by an access P-N diode, a bipolar junction transistor (BJT), or other suitable transistor. It should be appreciated that chalcogenide device 106 functions as a memory device.

[0016] Figure 3 is a normalized current (I)-normalized voltage (V) curve where different programming pulses were applied to applied to a threshold changing material in order to define different threshold voltages. As described in the above-mentioned related application (Attorney Docket No. MXICP020), the V_{th} of chalcogenide may be adjusted by applying energy into the film. Therefore, there may be different V_{th} within a single memory core cell. To program a cell, the steering transistor of the selected cell may be activated and a certain energy pulse is applied to the cell. The energy pulse is associated with a certain duration and profile. For example, to program a cell a voltage from 0.1 V to 20 V may be applied. In one embodiment, the duration may be 1 nanosecond (ns) to 1000 ns. One skilled in the art will appreciate that different programming pulses result in different V_{th}. The various states illustrated in Figure 3 are associated with the four threshold voltages (V_{th}). That is, V_{th1} is associated with a first state, V_{th2} is associated with a second state, V_{th3} is associated with a third state, and V_{th4} is associated with a fourth state.

[0017] Table 1 below provides a truth table associated with the four states illustrated in Figure 3. As can be seen, state 1 is defined when the read voltage V_a is between V_{th1} and V_{th2}. States 1 and 2 are defined when the read voltage V_b is between V_{th2} and V_{th3}. States 1, 2, and 3 are defined when the read voltage V_c is between V_{th3} and V_{th4}. States 1, 2, 3, and 4 are defined when the read voltage V_d is greater than V_{th4}.

TABLE 1

State	1	2	3	4
Read Voltage\V_{th}	V_{th1}	V_{th2}	V_{th4}	V_{th3}
$V_{th1}<V_a<V_{th2}$	On	Off	Off	Off
$V_{th2}<V_b<V_{th3}$	On	On	Off	Off
$V_{th3}<V_c<V_{th4}$	On	On	On	Off
$V_{th4}<V_d$	On	On	On	On

[0018] Figure 4 is a flow chart diagram illustrating the method operations for reading the multi-level states associated with a threshold changing material. The method initiates with decision operation 122 where a current is measured at read voltage V_b. If the current is high (on), then the method advances to operation 124 where the state is either state one or state two. The method then moves to decision operation 126 where the current is measured at read voltage V_a. If the current is high (on), then the associated state is state one as indicated in box 128. If the current measured in decision operation 126 is low (off), then this is an indication of state two 130. Returning to decision operation 122, if the current measured at V_b is low (off), then this is an indication of either state three or four as represented by box 132. The method then proceeds to decision operation 134 where the current is measured at voltage V_c. If the current measured at V_c is high (on), then this is an indication of state three 136. If the current measured at V_c is low (off), then the associated state here is state four as represented by box 138.

[0019] Figure 5 is a flowchart diagram of an alternative method for reading the multi-level states of a threshold changing material described with reference to Figure 4. The method initiates with a decision operation 140 where a current is measured at voltage V_a. If the current associated with read voltage V_a indicates high (on), then the method proceeds to operation 142 which indicates that the state is either state two, three or four. The method then proceeds to decision operation 144 where the current is measured at read voltage V_b. If the current associated with V_b is high (on), this indicates either state three or state four in box 146. The method then moves to decision operation 148 where the current is measured at voltage V_c. If the voltage at V_c is high (on), then state three is indicated as provided by box 150. If the current measured in decision operation 148 indicates low (off),

then this represents state four, box 156. If the current measured in decision operation 144 at V_b indicates low (off), then state two has been identified as represented by box 154. Returning to decision operation 140, if the current measured at V_a is low (off), then state one, box 152 has been achieved.

[0020] In summary, a multi-level chalcogenide memory is described herein. The multi-level data are stored according to different threshold voltages. In one embodiment, the threshold voltage is tuned by applying different energy pulses (further information on applying different energy pulses to tune the threshold voltage has been incorporated herein by reference). Additionally, two reading methods have been discussed. It should be appreciated in each of the reading methods the reading voltage should be higher than the threshold voltage. Accordingly, by changing the threshold voltage of the threshold changing material, a multi-level memory is provided. As discussed above, a multi-level non-volatile random access memory may be achieved in one embodiment of the invention. Since the reading sensing margin is very large ,as opposed to a resistance-based model, the multi-level stages may be easily discerned. Reading the current suffices to provide a distinguishing feature. Furthermore, the reading speed is relatively fast as compared to other reading speeds, i.e., the speed associated with reading resistance.

[0021] The invention has been described herein in terms of several exemplary embodiments. Other embodiments of the invention will be apparent to those skilled in the art from consideration of the specification and practice of the invention. The embodiments and preferred features described above should be considered exemplary, with the scope of the invention being defined by the appended claims and their equivalents.

Claims

1. A multilevel memory core, comprising:

   a word line;
   a bit line; and
   a core cell in electrical communication with the word line and the bit line, the core cell including a threshold changing material, the threshold changing material programmed to define multiple levels for storage, each of the multiple levels for storage associated with a corresponding threshold voltage.

2. The multilevel memory core of claim 1, further comprising:

   a steering element in electrical communication with the core cell.

3. The multilevel memory core of claim 2, wherein the steering element is an access transistor.

4. The multilevel memory core of claim 2, wherein the steering element is an access P-N diode.

5. The multilevel memory core of claim 2, wherein the steering element is an access bipolar junction transistor (BJT).

6. The multilevel memory core of claim 1, wherein each corresponding threshold voltage is different.

7. The multilevel memory core of claim 1, wherein each corresponding threshold voltage is associated with a corresponding current.

8. The multilevel memory core of claim 1, wherein the threshold changing material is a chalcogenide material.

9. The multilevel memory core of claim 1, wherein each level of the multilevel memory core defines a state, the state being detected by a current difference.

10. The multilevel memory core of claim 1, wherein the multilevel memory core is a nonvolatile random access memory.

11. A method for reading a multilevel memory device, comprising:

    applying a read voltage to the multilevel memory device;
    determining a state of a current associated with the read voltage; and
    determining an access state of the multilevel memory device based on the current.

12. The method of claim 11, wherein the read voltage is greater than a threshold voltage.

13. The method of claim 11, wherein the method operation of applying a read voltage to the multilevel memory device includes,

    applying a different read voltage to the multilevel memory device if the state of the current associated with the voltage is an on state.

14. The method of claim 11, further comprising:

    programming the multilevel memory device.

15. The method of claim 14, wherein the programming of the multilevel memory device includes:

    applying a voltage between about 0.1 volt and 20 volts.

16. The method of claim 15, wherein the applying of the voltage between about 0.1 volt and 20 volts includes:

applying the voltage for between about 1 nanosecond (ns) and 1,000 ns.

17. The method of claim 11, wherein the multilevel memory device is a nonvolatile memory device.

18. The method of claim 14, wherein the programming of the multilevel memory device includes:

activating a steering transistor.

19. A method for reading multiple levels of a multilevel memory device, comprising:

applying a voltage to a threshold changing material of the multilevel memory device; and
sensing a current related to the voltage to distinguish between each of the multiple levels.

20. The method of claim 19, further comprising:

applying an other voltage;
sensing a current related to the other voltage; and
calculating a current difference.

21. The method of claim 20, wherein the current difference is a difference between the current related to the voltage and the current related to the other voltage.

22. The method of claim 19, wherein the threshold changing material is a chalcogenide material.

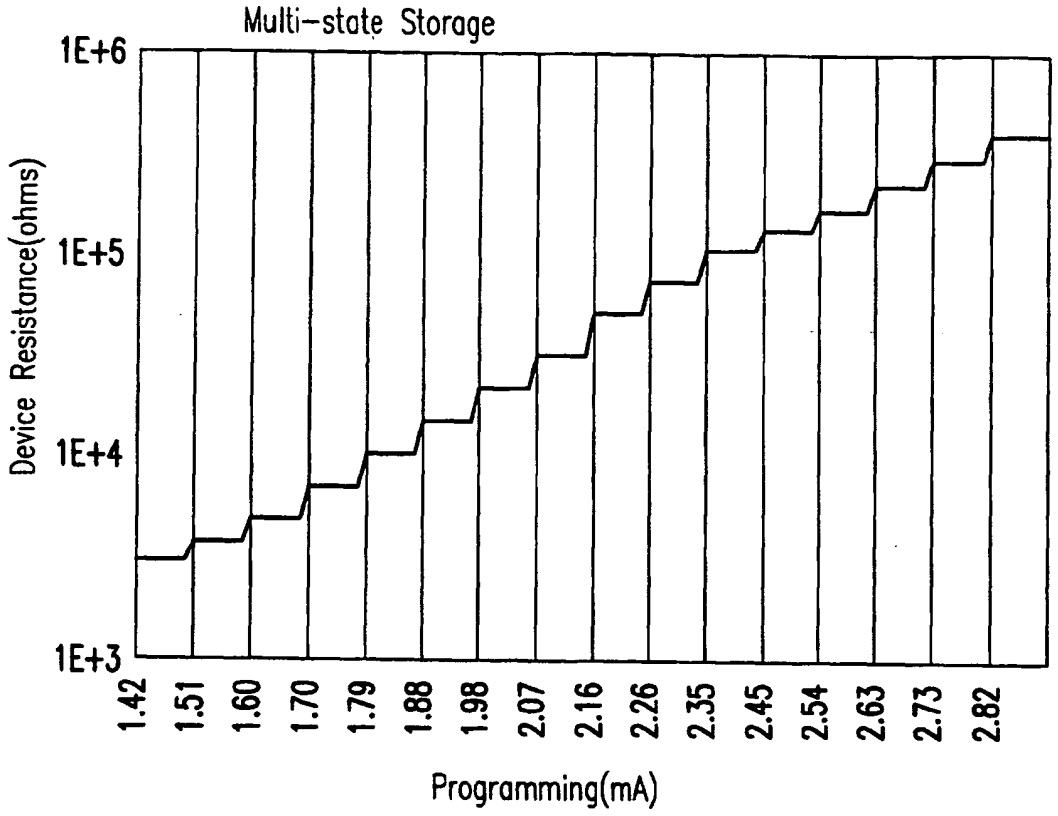

FIG. 1

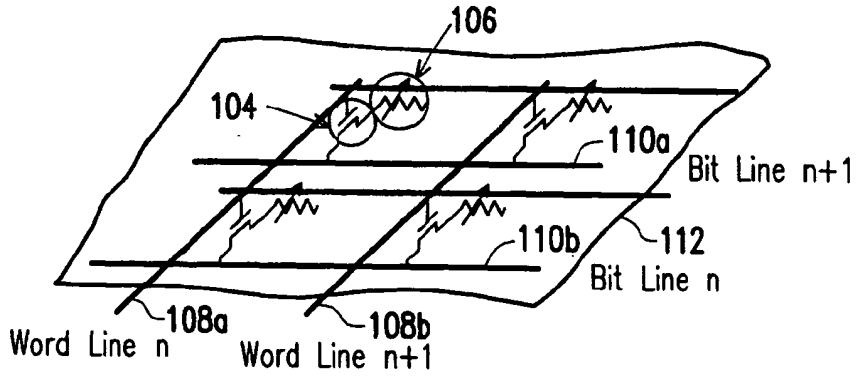

FIG. 2

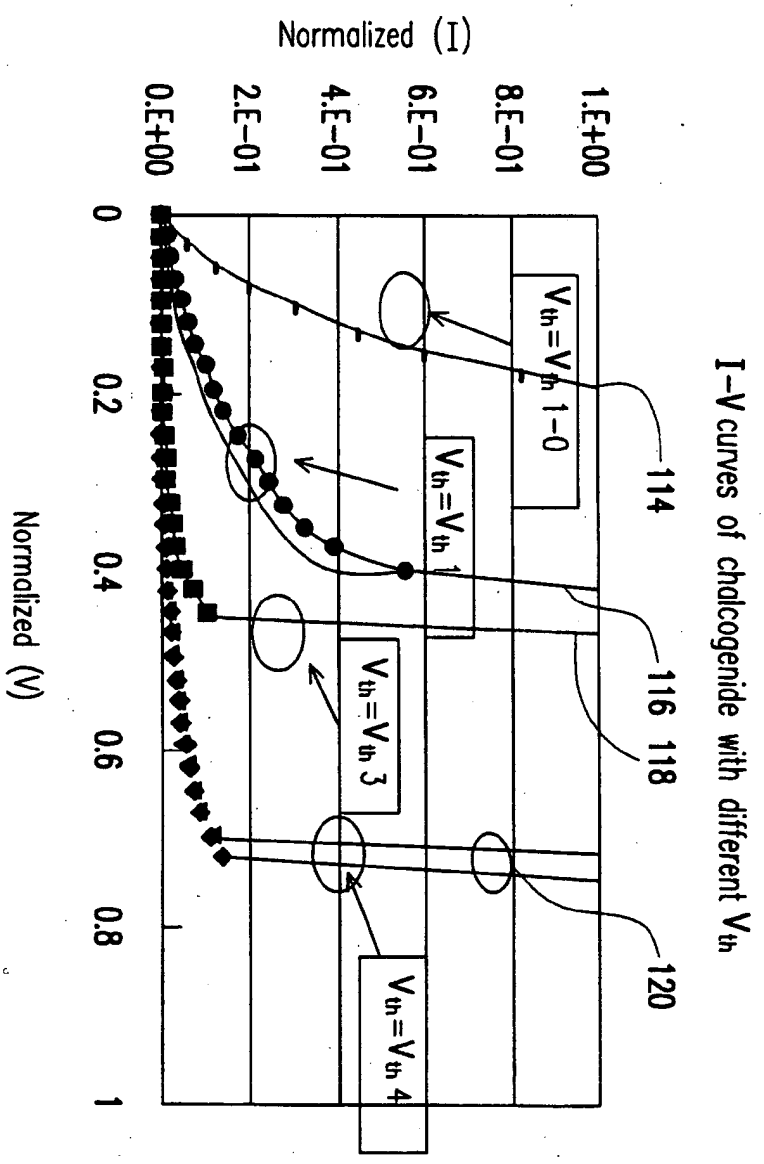

FIG. 3

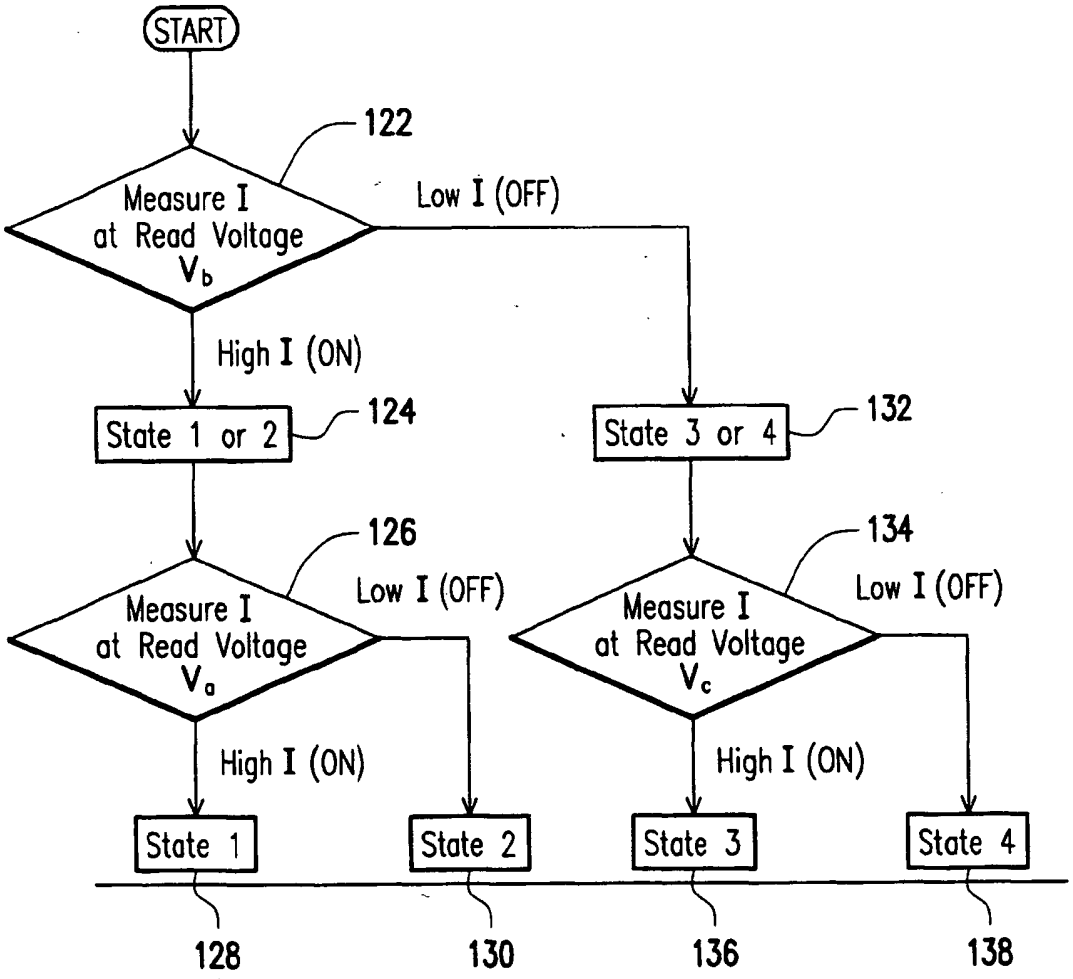

FIG. 4

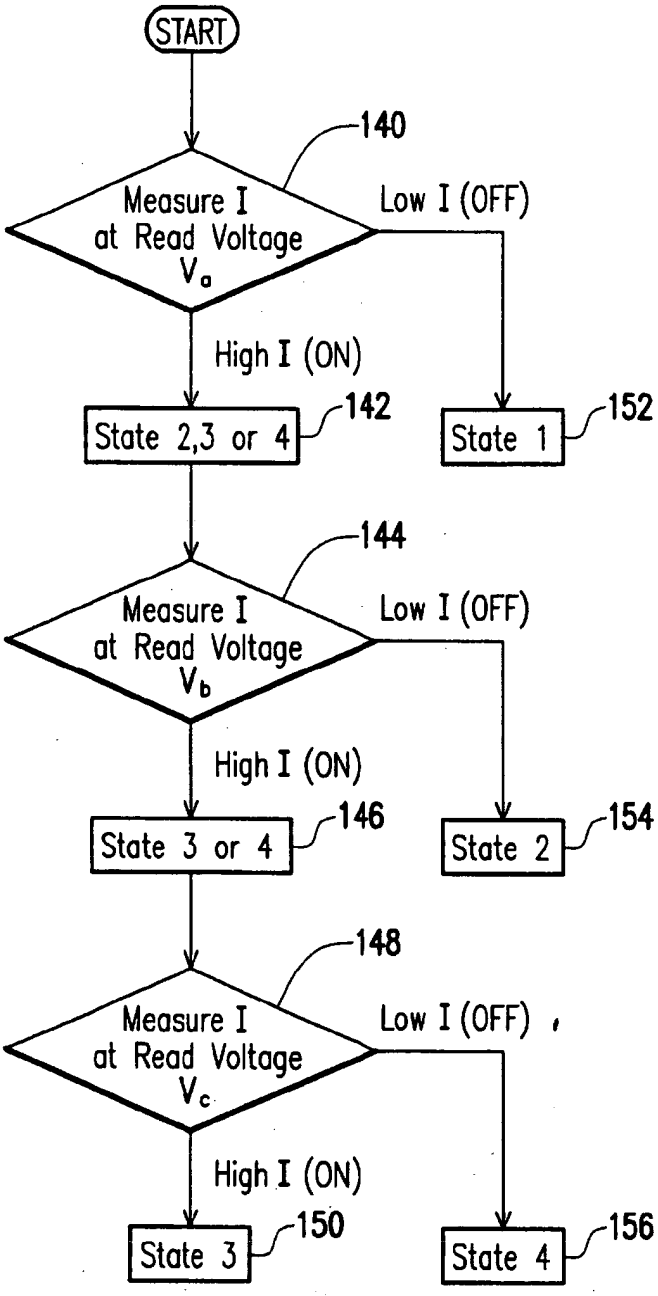

FIG. 5

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 03 02 6610

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
X Y	US 2003/067013 A1 (YODA HIROAKI ET AL) 10 April 2003 (2003-04-10) * paragraph [0091] - paragraph [0100] * * paragraph [0107] - paragraph [0110] * * figures 1,2 *	1-11, 14-19,22 12,13, 20,21	G11C11/56 G11C11/34
X	HWANG Y N ET AL: "Completely CMOS-Compatible Phase-Change Nonvolatile RAM Using NMOS Cell Transistors" NON-VOLATILE SEMICONDUCTOR MEMORY WORKSHOP,CA, USA, 16 February 2003 (2003-02-16), pages 91-92, XP002247864 * page 91, left-hand column, paragraph 2 - right-hand column, paragraph 4; figures 1,6,7 *	1,11,19	
X	US 2002/154531 A1 (LOWREY TYLER ET AL) 24 October 2002 (2002-10-24) * paragraph [0041] - paragraph [0071]; figures 2-4 *	1,11,19	TECHNICAL FIELDS SEARCHED (Int.Cl.7) G11C
Y	CALLIGARO C ET AL: "Dichotomic current-mode serial sensing methodology for multistorage non-volatile memories" CIRCUITS AND SYSTEMS, 1995., PROCEEDINGS., PROCEEDINGS OF THE 38TH MIDWEST SYMPOSIUM ON RIO DE JANEIRO, BRAZIL 13-16 AUG. 1995, NEW YORK, NY, USA,IEEE, US, 13 August 1995 (1995-08-13), pages 302-305, XP010165128 ISBN: 0-7803-2972-4	13,20,21	
A	* the whole document *	11,12,19	

-/--

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
The Hague	11 August 2004	Colling, P

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

European Patent Office

EUROPEAN SEARCH REPORT

Application Number
EP 03 02 6610

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
Y	US 4 199 692 A (NEALE RONALD G) 22 April 1980 (1980-04-22)	12	
A	* column 4, line 15 - column 5, line 9 *	14-22	
A	WO 96/10256 A (INTEL CORP) 4 April 1996 (1996-04-04) * page 9, line 1 - page 25, line 11; figures 1-9; table 1 *	1-7,9-21	
			TECHNICAL FIELDS SEARCHED (Int.Cl.7)

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
The Hague	11 August 2004	Colling, P

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

EPO FORM 1503 03.82 (P04C01)

ANNEX TO THE EUROPEAN SEARCH REPORT ON EUROPEAN PATENT APPLICATION NO. EP 03 02 6610

This annex lists the patent family members relating to the patent documents cited in the above-mentioned European search report. The members are as contained in the European Patent Office EDP file on
The European Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

11-08-2004

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 2003067013 A1	10-04-2003	JP 2003100085 A	04-04-2003
US 2002154531 A1	24-10-2002	US 6314014 B1	06-11-2001
		AU 2086101 A	25-06-2001
		WO 0145108 A1	21-06-2001
US 4199692 A	22-04-1980	NONE	
WO 9610256 A	04-04-1996	US 5508958 A	16-04-1996
		AU 3721595 A	19-04-1996
		CN 1166887 A ,C	03-12-1997
		DE 69521710 D1	16-08-2001
		DE 69521710 T2	08-05-2002
		EP 0783754 A1	16-07-1997
		HK 1001436 A1	22-02-2002
		JP 10507026 T	07-07-1998
		KR 263402 B1	01-08-2000
		WO 9610256 A1	04-04-1996

EPO FORM P0459

For more details about this annex : see Official Journal of the European Patent Office, No. 12/82